ECE/CS 552: Nanophotonics
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Nanophotonics
- Nanophotonics overview
  - Sharing the nanophotonic channel
    - Light-speed arbitration [MICRO 09]
  - Utilizing the nanophotonic channel
    - Atomic coherence [HPCA 11]

Good News
- Technology advances at astounding rate
  - 19th century: attempts to build mechanical computers
  - Early 20th century: mechanical counting systems (cash registers, etc.)
  - Mid 20th century: vacuum tubes as switches

Si
- 1965: Moore’s law [Gordon Moore]
  - Predicted doubling of IC capacity every 18 months
  - Drives functionality, performance, cost
    - Exponential improvement for 40+ years
    - Built on Von Neumann model (fetch/execute)

Distributed processing on chip
- Future chips rely on distributed processing
  - Many computation/cache/DRAM/IO nodes
  - Placement, topology, core arch/strength, ibd
- Conventional interconnects may not suffice
  - Buses not viable
  - Crossbars are slow, power-hungry, expensive
  - NOCs impose latency, power overhead
- Nanophotonics to the rescue
  - Communicate with photons
  - Inherent bandwidth, latency, energy advantages
  - Silicon integration becoming a reality
- Challenges & opportunities remain

Si Photonics: How it works
- Laser
  - Off-Chip Power
- Waveguide
  - Optical Wire
- Ring Resonator
  - Wavelength Magnet
  - ~3.5 μm
  - 0.5 μm
  - Ring Resonator [Koch '07]

Ring Resonators
Key attributes of Si photonics

- Very low latency, very high bandwidth
- Up to 1000x energy efficiency gain
- Challenges
  - Resonator thermal tuning: heaters
  - Integration, fabrication, is this real?
- Opportunities
  - Static power dominant (laser, thermal)
  - Destructive reads: fast wired or

Corona substrate [ISCA08]

- Targeting Year 2017
  - Logically a ring topology
  - One concentric ring per node
  - 3D stacked: optical, analog, digital

Multiple writer single reader (MWSR) interconnects

Motivating an optical arbitration solution

MWSR Arbiter must be:
1. Global - Many writers requesting access
2. Very fast – Otherwise bottleneck

Optical arbiter avoids OEO conversion delays, provides light-speed arbitration

Proposed optical protocols

- Token-based protocols
  - Inspired by classic token ring
  - Token == transmission rights
  - Fits well with ring-shaped interconnect
  - Distributed, Scalable
  - (limited to ring)

Baseline

- Based on traditional token protocols
- Repeat token at each node
  - But data is not repeated!
  - Poor utilization
**Optical arbitration basics**

<table>
<thead>
<tr>
<th>Token - Inject</th>
<th>Token - Seize</th>
<th>Token - Pass</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Token - Inject" /></td>
<td><img src="image2" alt="Token - Seize" /></td>
<td><img src="image3" alt="Token - Pass" /></td>
</tr>
</tbody>
</table>

- No Repeat!
- Token latency bounded by the time of flight between requesters.

**Arbitration solutions**

<table>
<thead>
<tr>
<th>Token Channel</th>
<th>Token Slot</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Token / Serial Writes</td>
<td>Multiple Tokens / Simultaneous Writes</td>
</tr>
</tbody>
</table>

**Flow control and fairness**

Flow Control:
- Use token refresh as opportunity to encode flow control information (credits available)
- Arbitration winners decrement credit count

Fairness:
- Upstream nodes get first shot at tokens
- Need mechanism to prevent starvation of downstream nodes

**Results - Performance**

| Uniform | HotSpot |

Token Slot benefits from:
- the availability of multiple tokens (multiple writers)
- fast turn-around time of flow-control mechanism

**Results - Latency**

| Uniform | HotSpot |

Token Slot has the lowest latency and saturates at 80%+ load

**Optical arbitration summary**

- Arbitration speed has to match transfer speed for fine-grained communication
  - Arbiter has to be optical
- High throughput is achievable
  - 85+% for token slot
- Limited to simple topologies (MWSR)
- Implementation challenges
  - Opt-elec-logic-elec-opt in 200ps (@5GHz)
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What makes coherence hard?

Unordered interconnects
- split transaction buses, meshes, etc
Speculation
- Sharer-prediction, speculative data use, etc.
Multiple initiators of coherence requests
- L1-to-L2, Directory Caches, Coherence Domains, etc
→ State-event pair explosion
- Verification headache

Example: MSI (SGI-Origin-like, directory, invalidate)

Stable States

Busy States

Races

"unexpected" events from concurrent requests to same block

Cache coherence complexity

L2 MOETSI Transitions

[Leppak Thesis, ’03]
Cache coherence verification headache

Verification

Formal Methods
e.g. Leslie Lamport’s TLA+

Papers:
So Many States, So Little Time:
Verifying Memory Coherence in the Cray X1 Complex Protocol

Simple

Complex Protocol

Verification

Atomic Coherence: Simplicity

w/ races

w/o races

Complex Verification

Simple

Race resolution

Cause:
Concurrently active coherence requests to block A

Remedy:
Only allow one coherence request to block A to be active at a time.

Core 0

$\text{CACHE}$

Core 1

$\text{CACHE}$

A

A

Race resolution

Core 0

$\text{CACHE}$

Core 1

$\text{CACHE}$

Atomic Substrate

Coherence Substrate

Atomic & Coherence Substrates

(Add speculation to a traditional protocol)

(Apply Fancy Nanophotonics Here)

Race resolution

Atomic Substrate

Coherence Substrate

Atomic Substrate

Coherence Substrate

--> Atomic Substrate is on critical path
+ Can optimize substrates separately

Atomic & Coherence Substrates
Mutexes circulate on ring

Single out mutex: hash(addr X) → λ, Y @ cycle Z

Mutex acquire

Exploits OFF-resonance rings: mutex passes P1, P2 uninterrupted

Mutex release

Mutexes on ring

Detectors Injectors

1 mutex = 200 ps = ~2cm = 1 cycle @ 5 GHz

# Mutex

Latency To:

• seize free mutex : ≤ 4 cycles
• tune ring resonator: < 1 cycle

Atomic Coherence: Complexity

Static:

Dynamic:

(random tester)

Performance

(128 in-order cores, optical data interconnect, MOEFSI directory)

Slowdown relative to non-atomic MOEFSI

What is causing the slowdown?

coherence agnostic
Optimizing coherence

Observation:
Holding Block B’s mutex gives holder free reign over coherence activity related to block B

**O.wned and F.orward State:**
- Responsible for satisfying on-chip read misses

Opportunity:
- Try to keep O/F alive
- If O (or F) block evicted:
  - While mutex is held, ‘shift’ O/F state to sharer
  - (or hand-off responsibility)

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Atomic Coherence Summary

- Nanophotonics as enabler
  - Very fast chip-wide consensus
- Atomic Protocols are simpler protocols
  - And can have minimal cost to performance (w/ nanophotonics)
  - Opportunity for straightforward protocol enhancements: ShiftF
- More details in HPCA-11 paper
  - Push protocol (update-like)

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