# ECE/CS 552: Introduction to Computer Architecture

Fall Semester 2010, MWF 2:25-3:15 EH2305, http://ece552.ece.wisc.edu

Instructor: Prof. Mikko Lipasti, mikko@engr.wisc.edu

TA: Guangyu Shi, gshi2@wisc.edu

## Course Description

**This course provides an introduction to the design of single-chip microprocessors and systems. Material covered in this course includes instruction set design, addressing, datapath design, control path design, pipelining, superscalar and out-of-order issue, multicore, memory management, caches and memory hierarchies, and interrupts and I/O structures.**

**Prerequisites for the course are ECE/CS 352 and ECE/CS 354.**

## Course Textbook

**D.A. Patterson and J.L. Hennessy, *Computer Architecture and Design: The Hardware/Software Interface, 4th* edition, Morgan Kauffman Publishers. If you cannot find the 4th edition, use the 3rd edition.**

## Homework

**There will be approximately 5 homework assignments which will not be weighted equally. Some assignments will require the review of material that is touched upon, but not covered in depth in class. Some homework assignments are to be completed inidividually, while for others you are expected to work in groups. No late homework will be accepted.**

## Project

**The project is to implement a working pipelined processor that implements the WISC-F10 instruction set. Extra credit will be granted for a more aggressive implementations, but only if the baseline pipelined implementation also works correctly. The project is to be completed in groups of three students; no individual projects will be allowed. Successful completion of the project includes a demonstration and a written report that documents your design.**

## Discussion Section

**There will be a weekly discussion section that meets in EH2540 on 5-6pm Mondays starting on 9/13/2010.**

## Examinations

**There will be an in-class midterm on 10/29 and a comprehensive final on Monday, Dec 20, at 12:25pm.**

## Grading

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|---|---|
| **Homework** | **20%** |
| **Midterm** | **30%** |
| **Final** | **30%** |
| **Project** | **20%** |

## Communications Channels

**I strongly encourage you to meet with me during my office hours, or call me or send e-mail. Introducing yourself to me, expressing concerns, offering suggestions, and seeking advice are among the welcome topics. Make sure you monitor the web site for this course which contains course information, lecture notes, pointers to project resources, and the latest announcements.**

# Office Hours

**Prof. Lipasti: EH4613, M3:30-4:30, R11-12**

**TA: Guangyu Shi, B622, W10:30-11:10, F2:30-3:30**

# Course Outline

| Week | Dates | Assignments | Topics | Readings |
|---|---|---|---|---|
| 0 | 9/3 | | Introduction | Ch 1 |
| 1 | 9/8,9/10 | HW1 out | Performance and Cost | Ch 1.4 |
| 2 | 9/13,9/15,9/17 | | Instruction Sets | Ch 2 |
| 3 | 9/20,9/22,9/24 | HW1 due, HW2 out | Arithmetic I | Ch 3.1-3.2 |
| 4 | 9/25,9/29,10/1 | | Datapath design | Ch 4.1 - 4.3, App C |
| 5 | 10/4,10/6,10/8 | HW2 due, HW3 out | Control | Ch 4.4, App C |
| 6 | 10/11,10/13,10/15 | Project out | Pipelining | Ch 4.5-4.9 |
| 7 | 10/18,10/20,10/22 | HW3 due | Intro to Superscalar | Ch 4.10-4.11, MIPS R10K paper |
| 8 | 10/25,10/27,10/29 | | Review and Midterm 10/29 | |
| 9 | 11/1,11/3,11/5 | HW4 out | Memory Technology | Ch 5.1, Slides |
| 10 | 11/8,11/10,11/12 | HW4 due, HW5 out | Memory Hierarchies | Ch 5.2 - 5.5 |
| 11 | 11/15,11/17,11/19 | | Memory Hierarchies cont'd | Ch 5.2 - 5.5 |
| 12 | 11/22,11/24 | HW5 due | Arithmetic II | Ch 3.3 - 3.5 |
| 13 | 11/29,12/1,12/3 | | I/O | Ch 6 |
| 14 | 12/6,12/8,12/10 | Project report due 12/10<br>Project demoe 12/12 | Parallel processing | Ch 5.7-5.9, Ch. 7 |
| 15 | 12/13,12/15 | | Review | -- |
| 16 | 12/20 | | Final Exam, 12:25pm Monday | -- |